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APPLICATION

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TITLE: DEVICE TESTING USING A HOLDING-CIRCUIT

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DEVICE TESTING USING A HOLDING-CIRCUIT

BACKGROUND

This invention relates to device testing using a holding-circuit.

When a new device is designed, it typically is tested to verify that the device conforms to design specifications. Testing is accomplished by applying input-signals to the device under test (DUT) and measuring the response-signals that result from the input-signals. In some testing environments, the input-signals are generated using a pulse-generating-source capable of producing pulse waveforms with pulse-widths in the nano-second range and rise-times in the pico-second range.

As the input-signals are applied to the DUT, measurements are taken at particular points on the DUT. To evaluate how the DUT responded to the input-signals, the response-signals and the input-signals are analyzed using standard measurement equipment. However, preserving input-signals for subsequent measurement purposes is difficult when the input-signals have narrow pulse-widths and fast rise-times.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 is a block diagram of a testing and measurement system.

FIG. 2 is a method of measuring a DUT.

FIG. 3 is a schematic diagram of a holding-circuit.

FIG. 4 is a timing diagram of signals in the holding-circuit.

DETAILED DESCRIPTION

As shown in FIGS. 1 and 2, a DUT 11 can be tested in a testing and measurement system 19. A pulse-generator 10 generates 100 event-signals 14a, 14n on line 14 and trigger-signals 16a, 16n on line 16. A model 4050B Pulse-generator manufactured by Picosecond Pulse Labs can be used as the pulse generator 10. A holding-circuit 13 receives the event-signals 14a, 14n, and trigger-signals 16a, 16n, and generates 102 output-signals 17a, 17n on line 17. DUT 11 receives the output-signals 17a, 17n and produces 104 buffered-output-signals 18a, 18n on line 18 and response-signals 15a, 15n on line 15. The measurement equipment 12 measures 106 the response of the DUT 11 based on the (1) buffered-output-signals 18a, 18n, and (2) response-signals 15a, 15n. The Tektronics DTS 694C oscilloscope can be used as the measurement equipment 12.

FIG. 3 shows a holding circuit 13 that includes a driving-circuit 35 and an impedance-network 36. The impedance-network includes a high-impedance-conductor 27 and a second-conductor 29. The holding-circuit 13 includes a third-conductor 21, a matching network 22, a sequential-logic-circuit 23, a reset-circuit 28, and a tri-state-buffer 26.

A trigger-signal feeds a trigger-port 20 such as a sub-miniature A connector (SMA). The trigger-signal can be, for example, in the 10-volt range. The trigger-port 20 is coupled to one end of a first-conductor 21 such as a 50-ohm microstrip that includes a 50-ohm trace with a width of about 0.045 inches using a 0.031-inch thick fire rating number 4 (FR4) board. Other designs can be used for the conductor 21 as well.

The other end of the first-conductor 21 is coupled to a matching-circuit 22 such as a voltage-divider that includes resistors R1 and R2. The ratio of R1/R2 produces a 50-ohm termination for the trigger-port 20. The matching-circuit 22 also translates the trigger-signal 16a to a level compatible with the holding-circuit 13.

The other end of the matching-circuit 22 is coupled to the clock-input 23a of a sequential-logic-circuit 23 such as a standard D-flip-flop. The data-input 23b of the sequential-logic-circuit 23 is connected to a voltage source (VCC) that

provides power for the holding-circuit 13. The value of VCC 25 can be set, for example, to a voltage in the range from 1.0 to 3.6 volts. VCC can be adjusted to match the high-value of the trigger-signal which corresponds to the logical-value of the trigger-signal 16a when it is close to VCC. The low-value of the trigger-signal corresponds to the logical-value of zero. This adjustment allows the level of a holding-signal generated by the holding-circuit 13 to match the level of the trigger-signal 16a. The voltage level of VCC also should be selected to match the signal levels used by the DUT 11.

When the trigger-signal 16a arrives at the clock-input 23a of the sequential-logic-circuit 23, it causes the Q-output 23d to be set to the high-value. The reset-input (RST) 23c of the sequential-logic-circuit 23 is coupled to a switch-circuit 28 such as a momentary contact switch. The switch-circuit 28 allows the signal level of the Q-output 23d to be reset to the low-value when the switch 28a is momentarily closed in the reset-position. During normal operation, the switch-circuit 28 is in the open position as shown in FIG. 3.

The tristate-enable 26a of a tristate-buffer 26 is coupled to and controlled by the Q-output 23d of the sequential-logic-circuit 23. In other implementations, a PMOS pull-up circuit can be substituted for the tristate-buffer 26. The tristate-input 26b is coupled to VCC, and the tristate-

output 26c is coupled to one end of a high-impedance-microstrip 27. The tristate-buffer 26 is enabled when the tristate-enable 26a receives a high-value signal. That causes the buffer 26 to have a high-value signal at the tristate-output 26c. In contrast, the tristate-buffer 26 is disabled when the tristate-enable 26a is set to the low-value. In the disabled state, the tristate-output 26c is in a high-impedance state.

The high-impedance-conductor 27 can be designed, for example, using a 150-ohm microstrip with a trace width of about 0.002 inches on an FR4 board with a thickness of about 0.031 inches. The other end of the high-impedance-conductor 27 is coupled to a tap point 32 along a second conductor 29. Other designs can be used for the conductor 27 as well.

One end of the second conductor 29 is coupled to an event port 31, and the other end of the second conductor is coupled to an output port 33. An event-signal feeds the event-port 31 which can be implemented, for example, using a standard SMA-type connector. Output-port 33 also can be implemented, for example, using a standard SMA-type connector. The second-conductor 29 can be implemented as a low-impedance microstrip using a 50-ohm trace with a width of about 0.045 inches on and FR4 board with a thickness of about 0.031 inches. Other designs can be used for the conductor 29 as well.

FIG. 4 shows an example of an event-signal 50 with a pulse-width w of about 250 nano-seconds that feeds the event-port 31 of the holding-circuit 13. The minimum pulse-width (w) is based on the propagation delay of components of the holding-circuit 13 and in this embodiment is about 25 nano-seconds. The rising-edge 50r of the event-signal 50 has a rise-time of approximately 100 pico-seconds, although the holding-circuit 13 can operate with an event-signal 50 with a rising-edge 50r as long as 200 pico-seconds. In other embodiments, the holding-circuit 13 is able to operate with a rising-edge 50r as small as 45 pico-seconds based on the specifications of the Model 4050B Pulse-generator. The fall-time of the falling-edge 50f is not critical.

A trigger-signal 51 which is synchronized with the event-signal 50 is fed simultaneously to the trigger-port 20 of the holding-circuit 13. The rising-edge 51r of the trigger-signal 51 should occur within the time-interval between the rising-edge 50r and the falling-edge 50f of the event-signal 50.

As the trigger-signal 51 arrives at the clock-input 23a of the sequential-logic-circuit 23, the rising-edge 51r causes a high-value Q-output-signal 52 with a propagation-delay of about 12 nano-seconds to appear at the Q-output 23d. The Q-output-signal 52 enables the tri-state-buffer 26 which

generates a holding-signal 53 that drives the high-impedance-conductor 27 having a high-value.

By applying the holding-signal 53 to the high-impedance-conductor 27, the event-signal 50 is captured as shown by output-signal 55. The state of the output-signal 55 is maintained even after the event-signal 50 changes to a different state. For example, as the event-signal 50 changes to a different state - as shown by the falling-edge 50f - the output-signal 55 is maintained at the high-value of the event-signal 50 even after the event-signal 50 returns to the low-value. The output-signal 55 appears at the output-port 33 after a propagation-delay of approximately 150 pico-seconds. The removal of the event-signal 50 causes a slight dip 63 to occur at the output-signal 55 due to the combined transmission and capacitive effects of the second-conductor 29 and the high-impedance-conductor 27.

The output-signal 55 can be reset to a low-value by closing the switch 28a to place the switch-circuit 28 in the reset-position. That causes a reset-signal 54 to be generated which feeds the rst-input 23c of the sequential-logic-circuit 23 and causes the Q-output-signal 52 to be reset 64 to the low-value. The signal 52 is fed to the enable input 26a of the tristate-buffer 26 which disables the tristate-buffer 26, as indicated by 67. After a slight propagation-delay, the

output-signal 55 returns to the low-value. The holding-circuit 13 can perform a subsequent holding operation.

The values of the particular signals discussed above are intended as examples only. Signals having different values can be used in other implementations.

The foregoing techniques can enable a high rise-time signal to be captured and held for subsequent test measurement purposes. The holding-circuit requires few electronic components, thereby providing a cost-effective technique.

In some implementations, a blocking-capacitor can be used between the pulse-generator 10 and the trigger-port 20 to protect the circuitry of the holding-circuit 13. Other implementations are within the scope of the following claims.